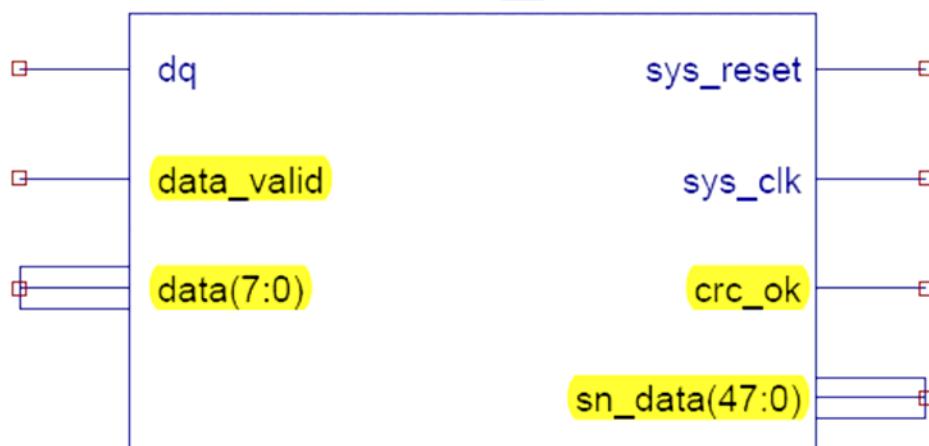


```
-----
-- DESCRIPTION :
-- Interface for the Silicon Serial Number Device DS2401 through a 1-Wire Bus.
--
-- It will output the data from the DS2401 byte by byte while data_valid is
-- asserted. Totally 8 bytes of data will show up on the data bus in sequence of:
--   Family code (x01 for DS2401) : 1 byte
--   Serial number (e.g. xABCDEF) : 6 bytes
--   CRC value (based on polynomial = x^8 + x^5 + x^4 + 1) : 1 byte
--
-- The Serial number appears in sn_data after completion of the sequence.
--
-- It connects to the DS2401 through only one wire (dq), which is a bidirectional
-- data path with internal pullup resistor (about 13KOhm, which is higher than the
-- specification of 5KOhm on the DS2401 datasheet) or an external pull-up resistor.
--
-- It uses a clock divider to generate a slow clock (1MHz) for the 1-Wire Master
-- module from the system clock. Use a generic (CLK_DIV) to specify the divider
-- ratio for different input clock rate.
--
-- It generates a crc_ok signal which indicates all the data have been received/output
-- and crc checking is OK if the generic (CheckCRC) is turned on.
--
-- THE ORIGINAL SOURCE FOR THIS MODULE AND ITS SUB-MODULES IS THE XILINX WEB REPOSITORY.
-- REFERENCE: APPLICATION NOTE "XAPP198" FROM www.xilinx.com
-----
-- IMPLEMENTATION NOTES :
-- The ports required to connect this module in your specific top level are:
--   SYS_CLK: connect to system clock.
--   SYS_RESET: connect to a strobe signal (active high) to trigger readout.
--             If tied to VCC, readout will start automatically when sys_clk is turned on.
--   CRC_OK: connect to a bit in the status word.
--   SN_DATA: connect to the corresponding input (48 bits) for the SSN on your Personality module
--   DQ: connect to the corresponding pin that goes to the DS2401 chip (bi-directional)
--
-- The other two ports (DATA, DATA_VALID) can be left unconnected.
--
-- Files required for this module:
--   + clk_div.vhd
--   + onewire_master.vhd
--   + shreg.vhd
--   + bitReg.vhd
--   + byteReg.vhd
--   + crcreg.vhd
--   + jcounter.vhd
-----
```

onewire_iface



4/5/2006

```
generic (
    CLK_DIV : integer range 0 to 15 := 9; -- Clock Divider for 40MHz system clock input
    ADD_PULLUP : boolean := true; -- Add a pullup on the 1-Wire bus
    CheckCRC : boolean := true; -- Turn on/off CRC Generator
    UseDummy : boolean := false -- Outputs dummy value for sn_data (instead of the real
value)
);

sys_clk      : in std_logic;      -- system clock (40Mhz)
sys_reset    : in std_logic;      -- active high syn. reset
data         : out std_logic_vector(7 downto 0); -- data output
data_valid   : out std_logic;     -- data output valid (20us strobe)
crc_ok       : out std_logic;     -- crc ok signal (active high)
sn_data      : out std_logic_vector(47 downto 0) -- parallel output
dq          : inout std_logic;   -- connect to the 1-wire bus

reset_i <= sys_reset;
crc_ok  <= crcok;
```